Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte QWAI H. LOW, CHOK J. CHIA, and SENG-SOOI LIM

Appeal No. 2001-1019
Application No. 08/928,826

ON BRIEF

Before THOMAS, DIXON, and LEVY, **Administrative Patent Judges**.

DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 14-19, which are all of the claims pending in this application.

We REVERSE.

BACKGROUND

Appellants' invention relates to an integrated circuit package which is packaged in a programmable manner to connect vias to conductors after mounting of the integrated circuit die on a circuit board . An understanding of the invention can be derived from a reading of exemplary claim 14, which is reproduced below.

14. A method for manufacturing an integrated circuit apparatus for electrically connecting a plural number of connection pads on an integrated circuit die to external connection pads, the method comprising the steps of:

mounting an integrated circuit die on a connector board, the connector board including;

a central region on a first surface thereof and a plural number of external connection pads disposed in a selected pattern on an opposite surface of the connector board;

a plurality of individual conductive finger connections disposed on the first surface of the connector board in laterally-spaced array about the central region for forming wire connections thereon;

a plural number of conductive vias disposed in electrical contact with the external connection pads and traversing the spacing between said first and said opposite surfaces of the connector board and being electrically connected to selected ones of the finger

connections for providing electrical continuity between selected finger connections and selected external connection pads;

a first conductor on the first side of the connector board, the first conductor not being electrically connected to any of the conductive vias;

after the step of mounting the integrated circuit die on the connector board, connecting a first one of the finger connections to the first conductor, thereby electrically connecting the first conductor with one of the conductive vias that is connected to the first one of the finger connections, thereby establishing whether the first conductor will be a power conductor or a ground conductor; and

after the step of mounting the integrated circuit die on the connector board, connecting at least two bond pads on the integrated circuit with the first conductor.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Mallik et al. (Mallik)	4,891,687	Jan. 02, 1990
Dehaine et al. (Dehaine)	4,982,311	Jan. 01, 1991
Chia et al. (Chia)	5,841,191	Nov. 24, 1998 (filed Apr. 21, 1997)

Claims 14-19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Dehaine in view of Mallik and Chia.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 22, mailed Nov. 21, 2000) for the examiner's reasoning in support of the rejections, and to appellants' brief (Paper No. 21, filed Oct. 23, 2000) for appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by appellants and the examiner. As a consequence of our review, we reverse, for the reasons set forth by applicants.

Appellants argue that none of the prior art shows the programming of the conductors which is a critical feature of the invention. (See brief at page 3.) We agree with appellants. While the language of independent claim 14 does not use this express language of "programming" as the examiner correctly points out in the answer, the instant claim is directed to a "method of manufacturing an integrated circuit . . ." where the claim recites that the conductors are not connected at the time of mounting and thereafter they are connected to a conductor on the circuit using the vias. Therefore,

we agree with appellants that the method steps with the associated states of the corresponding structure before and after mounting is changed which would be programming or configuring of the circuit after the mounting of the integrated circuit, to provide a modifiable interconnect pattern.

From our review of the examiner's answer, the examiner does not appear to appreciate that the claim is directed to a process of manufacturing rather than an article of manufacture. The examiner maintains that the end resulting structure is taught and fairly suggested by the combination of prior art teachings, and we tend to agree with the examiner. But the claim is directed to a process of manufacturing rather than an article of manufacture which the examiner has not addressed or explicitly pointed out where or how the prior art teaches the claimed mounting and then connecting the conductors and fingers to the vias as recited in independent claim 14.

Therefore, the examiner has not established a ***prima facie*** case of obviousness of the claimed invention, and we cannot sustain the rejection of independent claim 14 and its dependent claims 15-19.

CONCLUSION

To summarize, the decision of the examiner to reject claims 14-19 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)
JOSEPH L. DIXON Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)

jld/vsh

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